Claim Amendments

Please amend claims 1, 43, 47, and 53 as follows:

Please cancel claims 4, 5, 50 and 51 as follows:

Listing of Claims

1. (currently amended) A semiconductor device comprising:

a substrate having a surface orientation of (100);

a gate electrode formed on the substrate;

Slim spacers formed on the top of the substrate adjacent the gate electrode, said Slim spacers thinned to expose portions of [[an]] underlying source/drain extension regions (SDE);

wherein source/drain regions are oriented having a source-to-drain axis along the <100> direction; and

at least one tensile-stress film over the gate electrode and Slim spacers wherein the tensile-stress film exerts a tensile stress at a magnitude of about 50 MPa to about 2 GPa.

2. (previously presented) The semiconductor device of claim 1, wherein the width of the Slim spacers is less than about 500 Angstroms.

3. (previously presented) The semiconductor device of claim 1,

wherein the gate electrode comprises a gate structure having a gate length of less than about 80 nanometers.

4. (canceled)

5. (cancelled)

Claims 6-20 (canceled)

21. (previously presented) A CMOS structure having a reduced S/D electrical resistance and increased charge carrier mobility in a channel region comprising:

a semiconductor substrate;

a gate structure formed overlying the semiconductor substrate comprising a gate electrode;

thinned spacers adjacent either side of the electrode comprising an oxide/nitride portion adjacent the electrode;

wherein the width of said thinned spacers is adjusted to control a subsequent stress exerted on a channel region underlying the gate

electrode;

wherein said thinned spacers have a top portion at about the same level as the top portion of the gate electrode;

wherein source/drain extension (SDE) regions comprising the semiconductor substrate extend beyond a maximum width of the spacers; and,

at least one stressed dielectric layer disposed overlying the gate structure including said thinned spacers to exert a stress through said thinned spacers on said channel region.

22. (previously presented) The CMOS structure of claim 21, wherein the at least one stressed dielectric layer is in one of tensile and compressive stress.

23. (previously presented) The CMOS structure of claim 21, wherein the at least one stressed dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

24. (previously presented) The CMOS structure of claim 21, further

comprising salicide portions comprising a portion of the SDE doped regions.

25. (previously presented) The CMOS structure of claim 21, wherein the gate structure gate length is less than about 80 nm.

26. (previously presented) The CMOS structure of claim 21, wherein the maximum width of the thinned spacers is less than about 500 Angstroms.

27. (previously presented) The CMOS structure of claim 21, wherein the maximum width of the thinned spacers is less than about 400 Angstroms.

28. (previously presented) The CMOS structure of claim 21, wherein the oxide portion comprises CVD silicon oxide.

29. (previously presented) The CMOS structure of claim 21, wherein the nitride portion is selected from the group consisting of CVD silicon nitride and CVD silicon oxynitride.

30. (previously presented) The CMOS structure of claim 21, wherein the thinned spacers comprises substantially vertical sidewalls.

claims 31-39 (canceled)

40. (previously presented) The semiconductor device of claim 1, wherein the gate electrode comprises a PMOS device.

41. (previously presented) The semiconductor device of claim 1, wherein the Slim spacers have a width that is less than the width of the SDE regions by greater than about 20 percent.

42. (previously presented) The semiconductor device of claim 1, further comprising salicide portions on the SDE regions.

43. (currently amended) The semiconductor device of claim [[4]] 1, wherein the tensile-stress film is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

44. (previously presented) The CMOS structure of claim 21, wherein the gate structure comprises a PMOS device and the stressed dielectric layer in tensile stress.

45. (previously presented) The CMOS structure of claim 21, further

comprising source/drain regions oriented having a source-to-drain axis along the <100> direction.

46. (previously presented) The CMOS structure of claim 21, wherein the thinned spacers have a width that is less than the width of the SDE regions by greater than about 20 percent.

47. (currently amended) A semiconductor device comprising:

a substrate having a surface orientation of (100);

a gate electrode formed on the substrate;

Slim spacers formed on the top of the substrate adjacent either side of the gate electrode, said Slim spacers thinned to control a channel stress;

wherein source/drain regions are oriented having a source-to-drain axis along the <100> direction; and,

wherein at least one dielectric tensile-stress film is provided over the gate electrode and spacers exerting a tensile stress at a magnitude of about 50 MPa to about 2 GPa.

48. (previously presented) The semiconductor device of claim 47, wherein the width of the Slim spacers is less than about 500 Angstroms.

49. (previously presented) The semiconductor device of claim 47, wherein the gate electrode comprises a gate structure having a gate length of less than about 80 nanometers.

50. (canceled)

51. (canceled)

52. (previously presented) The semiconductor device of claim 47, wherein said slim spacers have a top portion at about the same level as the top portion of the gate electrode.

53. (currently amended) The semiconductor device of claim [[47]] 1, wherein said slim spacers have a top portion at about the same level as the top portion of the gate electrode.